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CRUTCHFIELD, CHRISTOPHER M	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,186	SCARR ET AL.	
	Examiner	Art Unit	
	Christopher M. Crutchfield	4144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *24 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/4/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. **Claims 1-4, 6-8, 20-25, 27-29 and 33** rejected under 35 U.S.C. 103(a) as being unpatentable over *Miles, et al.* (US Patent No. 6,665,495 B1) in view of *Li*, et al. (US Pre Grant Publication No. 2004/0066799 A1).

For Claim 1, *Miles, et al.* discloses a packet router comprising:

a. An input stage, (Figure 4, "Ingress Edge Units", Element 60) an output stage (Figure 4, “Egress Edge Units”, Element 160) and a coupling stage for coupling the input and output stages, (Figure 4, Elements 30, 32, 33, and 70) the input stage having plural input

devices each for receiving packets (Figure 4, Element 28, Figure 12a, Ports 1-16, Element 92 and Column 19, 5-7 and 18-19) having packet data comprising packet destination data, (Column 19, Lines 5-12) each input device having at least one output element (Figure 12a, Element 32).

b. The output stage having plural output devices defining plural router output nodes, (Figure 4, Elements 160 and 128 and Column 19, Lines 51-52) each output device having at least one input element (Figure 12b, Element 33).

c. The coupling stage providing paths for signals between the output elements of the input devices and the input elements of the output devices (Figure 4, Elements 30, 32, 33 and 70 and the Abstract).

d. Wherein each input device has circuitry arranged to respond to packet destination data of a packet received by the input device for adding, to the packet data of a *super packet*, information indicative of a router output node at which *a packet contained within the super packet* is to be output (Column 18, Lines 64-67 through Column 19, Lines 1-19 and Column 28, Lines 19-26 and Lines 29-33). (In each input device data are received from the various input ports [Figure 12a, Element 28] and is then classified by a classification module according to destination port and fed through a super packet processor [Figure 12a, Element 110] and ultimately to a super packet factory [Figure 12, Element 120] [Column 18, Lines 64-67 through Column 19, Lines 1-19] where packets destined for a single output port are grouped together and individual routing information

for each packet is appended to the super packet. [Column 28, Lines 19-26 and Lines 29-33 and Column 29, 58-64])

e. Wherein the router further comprises a control device connected to the input stage and to the coupling stage for causing packets to be output to the coupling stage in dependence on the packet destination data. (The packet classification module classifies a packet and assigns information indicative of a router output node to the packet and forewords the packet to the appropriate ingress super packet factory queue based on the assigned output port [Column 27, Lines 38-47 and Column 28, Lines 4-10 and 19-27] from which the packet is aggregated into a super packet and sent by the control device at the appropriate time [Column 21, Line 64 through Column 22, Line 6]. The control device/Super Packet Transmit Controller is connected to the input stage via the super packet ingress aggregator and the partial super packet ingress aggregator [See Figure 14]. The Control Device/Super Packet Transmit Controller is also connected to the core controller/coupling stage [Column 21, Lines 32-35].)

f. Wherein each output device has circuitry for removing the information prior to output of packets (Column 29, Line 65 to Column 30, Line 8). (The Classification index processing module of the egress module processes the output port indication from the super packet and then forewords the original packets accordingly [Column 29, Line 65 to Column 30, Line 8].)

g. Wherein the router further comprises a connecting device arranged to receive the signals from paths of the coupling stage and to transfer the signals to a further said output device disposed remote from the input stage (Column 25, Lines 50-61).

Miles, et al. does not disclose but *Li*, et al., from the same or similar field of endeavor, discloses each input device has circuitry arranged to respond to packet destination data of a packet received by said input device for adding, to the packet data of the packet, information indicative of a router output node at which the packet is to be output (Figure 4, Steps 401-435 and Column 3, Lines 24-37). (The ingress node of the network translates the addressing information into an internal label, which guides the packet to the egress node [Figure 4, Steps 401-435 and Column 3, Lines 24-37].) Thus it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to combine the packet indicators of *Li* et al. with the router network of *Miles, et al.* The packet indicators of *Li* et al. can be modified/implemented into the router network of *Miles, et al.* by having the super packet processor of *Miles, et al.* attach the packet destination data of each packet directly to each packet, as taught by *Miles, et al.*, instead of appending the destination data to the header of the super packet, and then having the egress module process the packets within the super packet based on the destination data stored in each packet instead of the super packet header. Therefore, claim 1 would have been obvious because the substitution the known element of a packet destination identifier stored in the header of a super packet for a destination identifier stored in the header of a packet is merely a substitution of one known element for another and would have yielded the predictable result of a router network that routes based on the contents of packet destination data stored within the packet to one of ordinary skill in the art at the time of the invention.

For Claim 2, *Miles, et al.* as modified by *Li*, et al. discloses each said input device has a plurality of inputs, (Figure 4, Element 28) a plurality of output elements (Column 8, Lines 13-15, See also Figure 17) and comprises a respective memory arranged to receive data from all of the said plurality of inputs and arranged to output data to all of said plurality of output elements (Figure 12a, Super Packet Factory, Figure 14, Element 124 and Column 20, Lines 8-11]) and wherein each output device has a plurality of input elements (Figure 4, Element 33, "DWDM Super Packet Link") and a plurality of router output nodes, (Figure 4, Element 128) and comprises a respective memory arranged to receive data from all of the said plurality of input elements and arranged to output data to all of said plurality of output nodes (Figure 12b, Super Packet Factory, Element 140 and Fig 15, Element 146). (Both the input device/ingress edge unit and the output device/egress edge unit have a memory forming a queue [Column 20, Lines 8-11 and Figure 14, Element 124 and Figure 15, Element 146] that receives data from the inputs [Figure 15, Element 33 and Figure 14, Element 108] and sends it to the respective outputs [Figure 14, Element 32 and Figure 15, Element 144]. The links to the core module/optical core comprise dense wavelength division multiplexed connections, and therefore comprise multiple output/input elements within a single fiber [Figure 14, Elements 128 and 32 and Figure 15, Elements 33 and 16].)

For Claim 3, *Miles, et al.* as modified by *Li*, et al. discloses the coupling stage (i.e. optical switch fabric) is arranged to vary the paths between the input stage and the output stage, (Column 12, Lines 24-34) and the control device (i.e. super packet processor) is arranged to cause packets to issue from the input stage when a desired path is provided (Column 21, Line 60 through Column 22, Line 17).

For Claim 4, *Miles, et al.* as modified by *Li*, et al. discloses said control device (i.e. super packet processor) is arranged to control the coupling stage (i.e. optical switch fabric/optical core

controller) to set up a desired path from the input stage to the output stage and to cause packets to issue from the input stage for the desired path (Column 21, Line 54 through Column 22, Line 17). (The super packet processor returns information such as queue depth and bandwidth demand to the optical core controller, which then arranges switching paths across the optical matrix accordingly, upon which the super packet processor transmits the data (Column 21, Line 54 through Column 22, Line 17).

For Claim 6, *Miles, et al.* does not disclose but *Li*, et al., from the same or similar field of endeavor, discloses the input devices comprise segmenting circuitry arranged to divide received packets into segments of common length prior to application to said coupling stage, wherein each segment includes the said router output node information of the packet and the output devices comprise desegmenting circuitry arranged to assemble segments received from said coupling stage into packets (Figure 4, Steps 410-435 and Column 3, Lines 24-37). Thus, it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to combine the common length segmentation of *Li*, et al. with the optical router of *Miles,* et al. The common length segmentation of *Li*, et al. can be modified/implemented into the optical router of *Miles,* et al. by replacing the super packet processor and the super packet factory of the ingress edge unit of *Miles, et al.* (*Miles,* Figure 12a, Elements 110 and 120) with the translating and segmenting functionality of *Li*, et al. (*Li*, Figure 4, Elements 405-415) and by replacing the super packet processor and the super packet factory of the egress module of *Miles,* et al. (*Miles,* Figure 12b, Elements 140 and 150) with the cell reassembling functionality of *Li*, et al. (*Li*, Figure 4, Elements 435). The motive to combine the common length segmentation of *Li*, et al. with the optical router of *Miles,* et al. is to allow the use of smaller individual cells of data within the switch, thereby eliminating the need to aggregate packets into a longer super packet to meet the minimum packet size of the switch, thereby eliminating the

need for large super packet buffers and reducing the necessary computing power to operate the switch.

For Claim 7, *Miles, et al.* as modified by *Li*, et al. discloses the input devices have optical output elements (Figure 12a, Element 32) and the output devices have optical input elements (Figure 12b, element 33) and the coupling stage is arranged to provide free-space optical paths between said optical output elements and optical input elements (Column 9, Lines 1-12 and Column 10, Lines 52-67).

For Claim 8, *Miles, et al.* as modified by *Li*, et al. discloses the connecting device (i.e. optical switch fabric) comprises a passive optical network (Column 9, Lines 1-12).

For Claim 20, *Miles, et al.* discloses a method of routing packets using a packet router comprising an input stage, (Figure 4, "Ingress Edge Units", Element 60) plural output devices (Figure 4, Element 128 and Column 19, Lines 51-52) and a coupling stage for coupling the input stage and output devices, (Figure 4, Elements 30, 32, 33, and 70) wherein at least one of the output devices is spatially remote from the coupling stage (Column 25, Lines 50-61) the method comprising:

a. In said input stage, examining packet destination data of a packet received by said input stage and in response thereto adding, to the *super packet*, router information indicative of a router output node of said at least one of said output devices, at which the packet is to be output to provide enhanced packet data (Column 18, Lines 64-67 through Column 19, Lines 1-19 and Column 28, Lines 19-26 and Lines 29-33). (In each input device data are received from the various input ports [Figure 12a, Element 28] and is then classified by a classification module according to destination port and fed through a super packet processor [Figure 12a, Element 110] and ultimately to a super packet

factory [Figure 12, Element 120] [Column 18, Lines 64-67 through Column 19, Lines 1-19] where packets destined for a single output port are grouped together and individual routing information for each packet is appended to the super packet. [Column 28, Lines 19-26 and Lines 29-33 and Column 29, 58-64])

b. In dependence on said router information, determining whether a path is available from an input of said coupling stage to an output connected to said at least one output device. (The packet classification module classifies a packet and assigns information indicative of a router output node to the packet and forewords the packet to the appropriate ingress super packet factory queue based on the assigned output port [Column 27, Lines 38-47 and Column 28, Lines 4-10 and 19-27] from which the packet is aggregated into a super packet and sent by the control device at a time when there is an available path to the indicated output node [Column 21, Line 64 through Column 22, Line 6].)

c. Outputting said enhanced packet data to said input of said coupling stage, whereby the enhanced packet data is carried to an output of said coupling stage for said at least one output device having the said router node. (The packet classification module classifies a packet and assigns information indicative of a router output node to the packet and forewords the packet to the appropriate ingress super packet factory queue based on the assigned output port [Column 27, Lines 38-47 and Column 28, Lines 4-10 and 19-27] from which the packet is aggregated into a super packet and sent by the control device over the switch core/coupling stage at a time when there is an available path to the indicated output node [Column 21, Line 64 through Column 22, Line 6].)

d. Receiving the enhanced packet data from said coupling stage output and transferring the packet data over a link (Column 25, Lines 50-61) to said at least one output device. (The output information enhanced super packet is received by an egress edge unit [Column 3, Lines 5-14].)

e. Receiving said enhanced packet data in the said output device and removing said router information. (The Classification index processing module of the egress module processes the output port indication from the super packet. [Column 29, Line 65 to Column 30, Line 8].)

f. Outputting said packet at said router output node. (The classification index forewords the packets to the destination egress port, where it is output. and then forewords the original packets accordingly [Column 29, Line 65 to Column 30, Line 8].)

Miles, et al. does not disclose but *Li*, et al., from the same or similar field of endeavor, discloses in said input stage, examining packet destination data of a packet received by said input stage and in response thereto adding, to *the packet*, router information indicative of a router output node of said at least one of said output devices (Figure 4, Steps 401-435 and Column 3, Lines 24-37). (The ingress node of the network translates the addressing information into an internal label, which guides the packet to the egress node [Figure 4, Steps 401-435 and Column 3, Lines 24-37].) Thus it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to combine the packet indicators of *Li* et al. with the router network of *Miles, et al.* The packet indicators of *Li* et al. can be modified/implemented into

the router network of *Miles, et al.* by having the super packet processor of *Miles, et al.* attach the packet destination data of each packet directly to each packet, as taught by *Miles, et al.*, instead of appending the destination data to the header of the super packet, and then having the egress module process the packets within the super packet based on the destination data stored in each packet instead of the super packet header. Therefore, claim 1 would have been obvious because the substitution the known element of a packet destination identifier stored in the header of a super packet for a destination identifier stored in the header of a packet is merely a substitution of one known element for another and would have yielded the predictable result of a router network that routes based on the contents of packet destination data stored within the packet to one of ordinary skill in the art at the time of the invention.

For Claim 21, *Miles, et al.* discloses a method of routing packets using a router (Abstract) comprising:

a. An input stage (Figure 4, "Ingress Edge Units", Element 60) having plural output elements, (Figure 14, Element 16 [There are 16 DWDM wavelengths for output]) plural output devices (Figure 4, Element 160) each having plural input elements, (Figure 15, Element 94 [There are 16 DWDM wavelengths for input]) the plural output devices each having a plurality of output nodes, (Figure 4, Element 128 and Column 19, Lines 51-52) said output nodes together defining the output nodes of said router, (Figure 12b, Element 128 and Column 19, Lines 36-52) and a coupling stage for coupling the plural output elements of the input stage to plural coupling stage outputs (Figure 4, Elements 30, 32, 33 and 70 and the Abstract).

b. Wherein at least one output device is spatially remote from the coupling stage (Column 25, Lines 50-61) and the router further comprises a link between predetermined outputs of said coupling stage and the plural inputs of said at least one output device (Figure 4, Elements 30, 32, 33 and 70 and the Abstract). (The input/output edge units may be located in spatially distinct areas, connected by a fiber link [Column 25, Lines 50-61].)

The method comprising:

i. Receiving respective packets at each of plural inputs of said input stage. (Abstract)

ii. In response to packet destination data of said packets, adding to each *super* packet respective router node information indicative of a router output node at which the said packet is to be output, thereby to form enhanced packet data comprising said packet data and said router node information (Column 18, Lines 64-67 through Column 19, Lines 1-19 and Column 28, Lines 19-26 and Lines 29-33). (In each input device data are received from the various input ports [Figure 12a, Element 28] and is then classified by a classification module according to destination port and fed through a super packet processor [Figure 12a, Element 110] and ultimately to a super packet factory [Figure 12, Element 120] [Column 18, Lines 64-67 through Column 19, Lines 1-19] where packets destined for a single output port are grouped together and individual routing information for each packet is appended to the super packet. [Column 28, Lines 19-26 and Lines 29-33 and Column 29, 58-64])

iii. Storing said enhanced packet data for each packet in a common input memory (Figure 12a, Super Packet Factory, Figure 14, Element 124 and Column 20, Lines 8-11]). (Both the input device/ingress edge unit and the output device/egress edge unit have a memory common to all packets held in that unit, forming a queue [Column 20, Lines 8-11 and Figure 14, Element 124 and Figure 15, Element 146] that receives data from the inputs [Figure 15, Element 33 and Figure 14, Element 108], stores it and sends it to the respective outputs [Figure 14, Element 32 and Figure 15, Element 144].)

iv. In dependence on said router node information indicative of an output node in said at least one output device, determining an available path through said coupling stage from an output element of said input stage to one of said predetermined outputs of said coupling stage. (The packet classification module classifies a packet and assigns information indicative of a router output node to the packet and forewords the packet to the appropriate ingress super packet factory queue based on the assigned output port [Column 27, Lines 38-47 and Column 28, Lines 4-10 and 19-27] from which the packet is aggregated into a super packet and sent by the control device to the appropriate output at the appropriate time when a path through the optical core is present [Column 21, Line 64 through Column 22, Line 6].)

v. Outputting said enhanced packet data from said common input memory to said output element, (Figure 14, Elements 126, 128 and 32) whereby the enhanced

packet data is carried to one of said predetermined outputs of said coupling stage. (The packet classification module classifies a packet and assigns information indicative of a router output node to the packet and forewords the packet to the appropriate ingress super packet factory queue based on the assigned output port [Column 27, Lines 38-47 and Column 28, Lines 4-10 and 19-27] from which the packet is aggregated into a super packet and sent by the control device at the appropriate over the optical core to the appropriate egress edge unit. [Column 21, Line 64 through Column 22, Line 6])

v. Transferring the enhanced packet data over said link [Column 21, Line 64 through Column 22, Line 6] to one of said plural inputs of said at least one output device (Column 3, Lines 5-15 Figure 4, elements 32, 30, 33, and 160)

v. Receiving said enhanced packet data at the said output device. (The output information enhanced super packet is received by an egress edge unit [Column 3, Lines 5-14].)

vi. Storing said packet data in a memory common to the input elements of said output device and to the output nodes of said output device (Figure 12a, Super Packet Factory, Figure 14, Element 124 and Column 20, Lines 8-11]). (Both the input device/ingress edge unit and the output device/egress edge unit have a memory common to all packets held in that unit, forming a queue [Column 20, Lines 8-11 and Figure 14, Element 124 and Figure 15, Element 146] that receives data from the inputs [Figure 15, Element 33 and Figure 14, Element

108], stores it and sends it to the respective outputs [Figure 14, Element 32 and Figure 15, Element 144].)

vii. Removing said router node information indicative of said output node to form packet data. (The Classification index processing module of the egress module processes the output port indication from the super packet. [Column 29, Line 65 to Column 30, Line 8].)

ix. Outputting a packet at said router output node from said memory (Figure 12a, Super Packet Factory, Figure 14, Element 124 and Column 20, Lines 8-11]). (Both the input device/ingress edge unit and the output device/egress edge unit have a memory common to all packets held in that unit, forming a queue [Column 20, Lines 8-11 and Figure 14, Element 124 and Figure 15, Element 146] that receives data from the inputs [Figure 15, Element 33 and Figure 14, Element 108], stores it and sends it to the respective outputs [Figure 14, Element 32 and Figure 15, Element 144].)

Miles, et al. does not disclose that the step of removing the router node information indicative of said output node to form packet data occurs before the packet is stored in the common memory. However, the use of separate packet queues within the memory to designate the output port is taught by *Miles*, et al. (See figure 15, Element 102, showing the output queues arranged by port). Thus it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention that the router node information could be removed from the super

packet prior to its storage in the queue and then output to the output ports based on its respective queue. Queue output indication can be modified/implemented in to the system of *Miles*, et al. by removing the router node information from received packets and re-constructing each packet and sending it to a specified port queue to be output to that port. The motive to combine Queue output indication with the system of *Miles*, et al. is to allow the output port to be designated by the queue, thus reducing the amount of processing necessary to output a packet in the queue to an output port.

Miles, et al. does not disclose but *Li*, et al., from the same or similar field of endeavor, discloses in response to packet destination data of said packets, adding to each *packet* respective router node information indicative of a router output node at which the said packet is to be output (Figure 4, Steps 401-435 and Column 3, Lines 24-37). (The ingress node of the network translates the addressing information into an internal label, which guides the packet to the egress node [Figure 4, Steps 401-435 and Column 3, Lines 24-37].) Thus it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to combine the packet indicators of *Li* et al. with the router network of *Miles, et al.* The packet indicators of *Li* et al. can be modified/implemented into the router network of *Miles, et al.* by having the super packet processor of *Miles, et al.* attach the packet destination data of each packet directly to each packet, as taught by *Miles, et al.*, instead of appending the destination data to the header of the super packet, and then having the egress module process the packets within the super packet based on the destination data stored in each packet instead of the super packet header. Therefore, claim 1 would have been obvious because the substitution the known element of a packet destination identifier stored in the header of a super packet for a destination identifier stored in the header of a packet is merely a substitution of one known element for another and would have yielded the predictable result of a router network that routes based on

the contents of packet destination data stored within the packet to one of ordinary skill in the art at the time of the invention.

For Claim 22, *Miles, et al.* as modified by *Li*, et al. discloses paths provided by said coupling stage (i.e. optical switch fabric) between the input stage and the output stage, (Column 12, Lines 24-34) and causing packets to issue from the input stage when a desired path is provided (Column 21, Line 60 through Column 22, Line 17).

For Claim 23, *Miles, et al.* as modified by *Li*, et al. discloses varying step comprises providing a sequence of path combinations, and selecting between said path combinations on a timed basis (Figure 7 and Column 13, Lines 26-30 and Column 31, Lines 47-53 and Column 32, Table 1). (A round robin schedule can be set up that varies equally each connection between the input and output in a repeating, time based pattern as shown by Table 1 [Column 32, Table 1] [Figure 7 and Column 13, Lines 26-30 and Column 31, Lines 47-53].)

For Claim 24, *Miles, et al.* as modified by *Li*, et al. discloses the varying step comprises providing a set of path combinations (Column 33, Table 3), and selecting between the members of said set in accordance with a statistical analysis of traffic in said router (Column 22, Line 60 Through Column 23, Line 11). (The optical core controller collects statistical information on each ingress edge unit [Column 22, Lines 60-65]. Using this information, the optical core controller provides a sequence of path combinations that can vary in order to maximize router throughput [Column 22, Line 60 through Column 23, Line 11].)

For Claim 25, *Miles, et al.* as modified by *Li*, et al. discloses controlling the coupling stage to set up a desired path from the input stage to the output stage and issuing packets from the input stage to the desired path (Column 21, Line 54 through Column 22, Line 17). (The super packet processor returns information such as queue depth and bandwidth demand to the optical core controller, which then arranges switching paths across the optical matrix

accordingly, upon which path arrangement the super packet processor transmits the data (Column 21, Line 54 through Column 22, Line 17).

For Claim 27, *Miles,* et al. does not disclose but *Li*, et al., from the same or similar file of endeavor, discloses comprising dividing received packets into segments of common length (Figure 4, Step 410) prior to application to said coupling stage, (Figure 4, Elements 420) and adding the said router node information to each segment (Figure 4, Step 415) (Figure 4, Steps 401-435 and Column 3, Lines 24-37). (The ingress node of the network splits each packet in to an equal length cell (Figure 4, Step 910) and then translates the addressing information into an internal label (Figure 4, Element 905) and affixes the label to each cell, (Figure 4, Element 915) which guides the individual to the egress node [Figure 4, Steps 401-435 and Column 3, Lines 24-37].) Thus it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to combine the packet splitting of *Li* et al. with the router network of *Miles, et al.* The packet splitting of *Li* et al. can be modified/implemented into the router network of *Miles, et al.* by having the super packet processor of *Miles, et al.* split packets to a designated cell length, as taught by *Miles, et al.*, instead of forming super packets, and then having the egress module re-assemble the packets upon receipt. The motive to combine fixed length cell routing with the system of *Miles, et al.* as modified by *Li*, et al. is to allow for the transmission of packets with a length that exceeds the maximum size of the super packet, therefore increasing the flexibility of the packet router.

For Claim 28, Miles, et al. as modified by Li, et al. discloses coupling between the input stage and the output devices using free-space optical paths (Column 11, Lines 20-31).

For Claim 29, Miles, et al. as modified by Li, et al. discloses the transferring step is carried out using a passive optical network (Column 11, Lines 20-31). (The data sent over the

optic core is transmitted over a simple optical crossbar which is a passive optical network, not actively reading any data in the optical packets [Column 11, Lines 20-31]).

4. **Claims 5 and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Miles, et al.* (US Patent No. 6,665,495 B1) and *Li*, et al. (US Pre Grant Publication No. 2004/0066799 A1) as applied to claims 1 and 21 above, and further in view of *Rodgers*, et al. (US Patent No. 6,147,991).

For Claim 5 and 26, *Miles, et al.* as modified by *Li*, et al. does not disclose but *Rodgers* et al. discloses that coupling stage is arranged to provide at least one fixed path. (Figure 2, Element 201 and Abstract). Thus, it would have been obvious to a person of ordinary skill in the pertinent art to combine the cross point matrix of *Rodgers* et al. with the router of *Miles, et al.* as modified by *Li*, et al. The cross point matrix of *Rodgers* et al. can be modified/implemented into the router of *Miles, et al.* as modified by *Li*, et al. by integrating the cross point matrix of *Rodgers,* et al. with the optical switch fabric of *Miles*, et al. [Figure 4, Element 30] and establishing direct connections between the ingress and egress edge units [*Miles*, Figure 4, Elements 60 and 160] for high traffic links. The motive to combine the cross point matrix of *Rodgers,* et al. with the router of *Miles, et al.* as modified by *Li*, et al. is provided by *Rodgers,* et al. and is to reduce bandwidth bottlenecks by allowing a direct connection between bust ports [*Rodgers,* Column 2, Lines 23-34].

5. **Claims 9 and 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Miles, et al.* (US Patent No. 6,665,495 B1) and *Li*, et al. (US Pre Grant Publication No. 2004/0066799 A1) as applied to claims 1 and 21 above, and further in view of *Battle,* et al. (US Patent No. 7,136,381).

For Claim 9, *Miles, et al.* as and by *Li*, et al. do not disclose but *Battle,* et al. discloses the input stage has a plurality of inputs capable of carrying a first plurality of packets to said router in a given time period, and the coupling stage is capable of providing said paths between said output elements of the input devices and said input elements of the output devices, wherein said paths are arranged to be able to carry more than said first plurality of packets in said given time. (Figure 1). (Each 8 port Gigabit ingress edge module switch contains 8 1 Gigabit ports and then connects via a 10 Gigabit core module to another 8 port Gigabit switch.) Thus, it would have been obvious to a person of ordinary skill in the pertinent art to include the over allocated ingress units of *Battle,* et al. in the switch of *Miles, et al.* as modified by *Li*, et al. The over allocated ingress units of *Battle,* et al. can be modified/implemented into the switch of *Miles, et al.* as modified by *Li*, et al. by increasing the number of wavelengths transmitted on the DWDM super packet link to such that the combined bandwidth exceeds that of the inputs to the ingress edge unit. The motive to combine the over allocated ingress units of *Battle,* et al. with the switch of *Miles, et al.* is provided by *Battle,* et al. and is to allow for expandability of the ingress edge units port density and to generally allow for higher speed transmission (Column 2, Lines 42-51).

Miles, et al. as and by *Li*, et al. and *Battle,* et al. and *Rodgers* et al. do not disclose that the ingress edge unit and core switch of *Rodgers* et al. could be optic. However, it is officially noted that the use of fiber optic cross ingress edge units and optical core switches was well known in the pertinent art at the time of the invention. Thus, it would have been obvious to a person of ordinary skill in the pertinent art to combine fiber optic cross ingress edge units and optical core switches with the system of *Miles, et al.* as modified by *Li*, et al. and *Rodgers* et al. Fiber optic cross ingress edge units and optical core switches can be modified/implemented into the system of *Miles, et al.* as modified by *Li*, et al. and *Rodgers* et al. by converting the cross point matrix to an optical cross point matrix. Thus, implementing a optic cross point matrix in the

cross point matrix of into the system of *Miles, et al.* as modified by *Li*, et al. and *Rodgers* et al. would have been obvious because the known technique of implementing a fiber optic switching matrix in place of a switching matrix was recognized as part of the ordinary capabilities of one skilled in the art.

For Claim 30, *Miles, et al.* as modified by *Li*, et al. does not disclose but *Battle,* et al. discloses carrying data across said coupling stage faster than said data is received at said input stage (Figure 1). (Each 8 port Gigabit ingress edge module switch contains 8 1 Gigabit ports and then connects via a 10 Gigabit core module to another 8 port Gigabit switch, thus allowing the data to cross the core switch matrix/coupling matrix at a speed faster then the data is received at the input stage [Figure 1]) Thus, it would have been obvious to a person of ordinary skill in the pertinent art to include the over allocated ingress units of *Battle,* et al. in the switch of *Miles, et al.* as modified by *Li*, et al. The over allocated ingress units of *Battle,* et al. can be modified/implemented into the switch of *Miles, et al.* as modified by *Li*, et al. by increasing the number of wavelengths transmitted on the DWDM super packet link to such that the combined bandwidth exceeds that of the inputs to the ingress edge unit. The motive to combine the over allocated ingress units of *Battle,* et al. with the switch of *Miles, et al.* is provided by *Battle,* et al. and is to allow for expandability of the ingress edge units port density and to generally allow for higher speed transmission (Column 2, Lines 42-51).

Miles, et al. as and by *Li*, et al. and *Battle,* et al. and *Rodgers* et al. do not disclose that the ingress edge unit and core switch of *Rodgers* et al. could be optic. However, it is officially noted that the use of fiber optic cross ingress edge units and optical core switches was well known in the pertinent art at the time of the invention. Thus, it would have been obvious to a person of ordinary skill in the pertinent art to combine fiber optic cross ingress edge units and optical core switches with the system of *Miles, et al.* as modified by *Li*, et al. Fiber optic cross

ingress edge units and optical core switches can be modified/implemented into the system of *Miles, et al.* as modified by *Li*, et al. and *Rodgers* et al. by converting the cross point matrix to an optical cross point matrix. Thus, implementing a optic cross point matrix in the cross point matrix of into the system of *Miles, et al.* as modified by *Li*, et al. and *Rodgers* et al. would have been obvious because the known technique of implementing a fiber optic switching matrix in place of a switching matrix was recognized as part of the ordinary capabilities of one skilled in the art.

6. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Miles, et al. (US Patent No. 6,665,495 B1), Li, et al. (US Pre Grant Publication No. 2004/0066799 A1) and Battle, et al. (US Patent No. 7,136,381) as applied to claim 9 above, and further in view of *Moriwaki*, et al. (US Patent No. 6,999,413).

For Claim 10, *Miles, et al.* as modified by and by *Li*, et al. and *Battle,* et al. does not disclose but *Moriwaki*, et al. from the same or similar field of endeavor, discloses a packet router wherein the number of spatially separate paths provided by said coupling stage is greater than the number of inputs to said input stage (Figure 1, Line I/F #1 has multiple spatially separate crossbar connections [10-1 to 10-n] to its single input). Thus, it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to include the multiple parallel crossbars of *Moriwaki*, et al. in the system of *Miles, et al.* as modified by *Li*, et al. and *Battle,* et al. The multiple parallel crossbars of *Moriwaki*, et al. can be modified/implemented into the system of *Miles, et al.* as modified by *Li*, et al. and *Battle,* et al. by installing and connecting to each ingress and egress module multiple parallel cross bar matrixes such that the number of crossbar matrixes exceeds the number of inputs to each ingress module. The motive to combine the multiple parallel crossbars of *Moriwaki*, et al. with the system of *Miles, et al.* as

modified by *Li*, et al. and *Battle,* et al. is provided by *Moriwaki*, et al. and is to allow for high capacity, expandability and fault tolerance (*Moriwaki*, Column 3 Lines 45-67).

Miles, et al. as modified by *Li*, et al., *Battle,* et al. and *Moriwaki*, et al. does not disclose that multiple parallel crossbars can be used in a multi stage switch where the number of inputs to an ingress edge module/Line I/F exceed one. However, it is officially noted that the use of multi stage switches was well known in the pertinent art at the time of the invention. Thus, it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention that multiple parallel crossbars exceeding the number of inputs could also be used in a multi stage switch where the ingress edge module/Line I/F has multiple inputs. Therefore, claim 10 would have been obvious because the technique for improving switches by installing multiple parallel crossbars exceeding the inputs to the ingress edge unit was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

Miles, et al. as modified by *Li*, et al., *Battle,* et al. and *Moriwaki*, et al. does not disclose that the ingress edge unit and core switch of *Moriwaki*, et al. could be optic. However, it is officially noted that the use of fiber optic cross ingress edge units and optical core switches was well known in the pertinent art at the time of the invention. Thus, it would have been obvious to a person of ordinary skill in the pertinent art to combine fiber optic cross ingress edge units and optical core switches with the system of *Miles, et al.* as modified by *Li*, et al., *Battle,* et al. and *Moriwaki*, et al. Fiber optic cross ingress edge units and optical core switches can be modified/implemented into the system of *Miles, et al.* as modified modified by *Li*, et al., *Battle,* et al. and *Moriwaki*, et al. by converting the cross point matrix to an optical cross point matrix. Thus, implementing a optic cross point matrix in the cross point matrix of into the system of *Miles, et al.* as modified by *Li*, et al., *Battle,* et al. and *Moriwaki*, et al. would have been obvious

because the known technique of implementing a fiber optic switching matrix in place of a switching matrix was recognized as part of the ordinary capabilities of one skilled in the art.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miles, et al. (US Patent No. 6,665,495 B1) and Li, et al. (US Pre Grant Publication No. 2004/0066799 A1) as applied to claim 1 above, and further in view of *Leonski*, et al. (US Patent No. 6,990,063).

For Claim 11, *Miles, et al.* discloses a network comprising a packet router wherein:

a. A packet router, the packet router having a router input stage, (Figure 4, "Ingress Edge Units", Element 60) a router output stage (Figure 4, “Egress Edge Units”, Element 160) and a router coupling stage for coupling the router input and output stages (Figure 4, Elements 30, 32, 33, and 70).

b. The router input stage has plural input devices each for receiving packets (Figure 4, Element 28, Figure 12a, Ports 1-16, Element 92 and Column 19, 5-7 and 18-19) having packet data comprising packet destination data, (Column 19, Lines 5-12) each router input device having at least one output element (Figure 12a, Element 32) and storage for holding queues of packet data prior to issue to the router coupling stage (Figure 14, Element 124 and 32).

c. The router output stage has plural output devices defining plural output nodes, (Figure 4, Element 128 and Column 19, Lines 51-52) each output device having at least one input element (Figure 12b, Element 33).

d. The router coupling stage is arranged to provide paths between the output elements of the input devices and the input elements of the output devices (Figure 4, Elements 30, 32, 33 and 70 and the Abstract).

Miles, et al. also further discloses that an output device of a packet router may be disposed remotely from said input stage of said first packet router (Column 25, Lines 50-61).

Miles, et al. and *Li*, et al. do not disclose the existence of a second router, (As shown in a-d, Supra) wherein the input devices of the second router input stage are provided by said further said output device of said packet router disposed remote from said input stage of said first packet router. However, the cascading of multiple routers was well known in the pertinent art at the time of the invention. Thus it would have been obvious that the remote output of a first router as described by *Miles,* et al. as modified by *Li*, et al. as presented in claim 1 above could be connected to the remote input of a second router as described by *Miles,* et al. (As shown in a-d, Supra). A second router as described by *Miles,* et al. can be connected to a first router as described by *Miles,* et al. as modified by *Li*, et al. by connecting the remote output of the first router *Miles,* et al. as modified by *Li*, et al. to the input of a second router as described by *Miles*, et al. The motive to combine a second router as described by *Miles,* et al. with a first router as described by *Miles,* et al. as modified by *Li*, et al. is to allow the use of multiple packet switches, therefore increasing bandwidth and the number of reachable destinations.

Miles, et al. and *Li*, et al. do not disclose, but *Leonski*, et al., from the same or similar field of endeavor discloses a second router input stage (Figure 1A, Element 115 and Figure 3B, Element 305) is provided by the output device of a packet router (Figure 1A, Element 110 and Figure 3A, Element 325) wherein each queue of packet data received from the coupling stage of the first packet router (Figure 1, Element 319) forms a queue of packet data (Figure 3A,

Element 320) for issue to the coupling stage of the second router (Figure 3A, Element 325 and Figure 1A, Element 115). (The first packet router/SE-1 takes input packets and distributes packets destined for the appropriate SE-2 stage/second router to an output queue [Figure 3A, Element 320] for that stage. The output of that output stage queue is then sent to the distribution stage of the SE-2/second router [Figure 3A, Elements 320, 325 and 328].) Thus it would have been obvious to a person of ordinary skill in the pertinent art that the single buffered router connection of *Leonski*, et al. could be combined with the system of *Miles, et al.* as modified by *Li*, et al. The single buffered router connection of *Leonski*, et al. can be modified/implemented into the system of *Miles, et al.* as modified by *Li*, et al. by removing the input buffer from the second router input stage that is connected to the remote first router output stage. The claim would have obvious because the substitution of the known element of a buffered router input stage for the element of an un-buffered router input stage would have been recognized by one of ordinary skill in the pertinent art at the time of the invention to yield the predictable result of cascaded routers connected by an un-buffered input.

8. **Claims 12-14 and 17-19** are rejected under 35 U.S.C. 103(a) as being unpatentable Miles, et al. (US Patent No. 6,665,495 B1) and *Leonski*, et al. (US Patent No. 6,990,063).

For Claim 12, *Miles, et al.* discloses a network comprising:

a. A router comprising an input stage (Figure 4, "Ingress Edge Units", Element 60) having plural input devices, (Figure 4, Element 28, Figure 12a, Ports 1-16, Element 92 and Column 19, 5-7 and 18-19) an output stage having plural output devices (Figure 4, Element 128 and Column 19, Lines 51-52) and a coupling stage for providing paths

between said input devices and said output devices (Figure 4, Elements 30, 32, 33 and 70 and the Abstract).

b. The input device having storage for holding queues of packet data (Figure 14, Element 124) prior to issue to said coupling stage, (Figure 14, Elements 126, 128 and 32) the output device having storage for queues of packet data (Figure 15, Element 146) received from the coupling stage (Figure 15, Elements 33, 136 and 138).

Miles, et al. does not disclose the existence of a second router, (As shown in a-b, Supra) wherein at least one of the input devices of the second packet router is provided by an output device of said first packet router. However, the cascading of multiple routers was well known in the pertinent art at the time of the invention. Thus it would have been obvious that the remote output of a first router as described by *Miles,* et al. as modified by *Li*, et al. as presented in a-b above could be connected to the remote input of a second router as described by *Miles,* et al. (As shown in a-b, Supra). A second router as described by *Miles,* et al. can be connected to a first router as described by *Miles,* et al. by connecting the remote output of the first router *Miles,* et al. to the input of a second router as of *Miles*, et al. The motive to combine a second router as described by *Miles,* et al. with a first router as described by *Miles,* et al. is to allow the use of multiple packet switches, therefore increasing bandwidth and the number of reachable destinations.

Miles, et al. does not disclose, but *Leonski*, et al., from the same or similar field of endeavor discloses at least one of the input devices of the second packet router (Figure 1A, Element 115 and Figure 3B, Element 305) is provided by an output device of said first packet router (Figure 1A, Element 110 and Figure 3A, Element 325) such that each queue of packet

data (Figure 1, Element 320) received from the coupling stage of the first packet router (Figure 1, Element 319) forms a queue of packet data (Figure 3A, Element 320) prior to issue to the coupling stage of the second router (Figure 3A, Element 325 and Figure 1A, Element 115). (The first packet router/SE-1 takes input packets and distributes packets destined for the appropriate SE-2 stage/second router to an output queue [Figure 3A, Element 320] for that stage. The output of that output stage queue is then sent to the distribution stage of the SE-2/second router [Figure 3A, Elements 320, 325 and 328].) Thus it would have been obvious to a person of ordinary skill in the pertinent art that the single buffered router connection of *Leonski*, et al. could be combined with the system of *Miles, et al.* The single buffered router connection of *Leonski*, et al. can be modified/implemented into the system of *Miles, et al.* by removing the input buffer from the second router input stage that is connected to the remote first router output stage. The claim would have been obvious because the substitution of the known element of a buffered router input stage for the element of an un-buffered router input stage would have been recognized by one of ordinary skill in the pertinent art at the time of the invention to yield the predictable result of cascaded routers connected by an un-buffered input.

For Claim 13, *Miles, et al.* as modified by *Leonski*, et al. discloses a network wherein:

a. Each said input device has a plurality of inputs (Figure 4, Element 28) and a plurality of output elements (Column 8, Lines 13-15, See also Figure 17) and a respective memory providing said storage for holding queues of packet data prior to issue to said coupling stage arranged to receive data from all of the said plurality of inputs and arranged to output data to all of said plurality of output elements (Figure 12a, Super Packet Factory, Figure 14, Element 124 and Column 20, Lines 8-11]). (Both the input device/ingress edge unit and the output device/egress edge unit have a memory forming

a queue [Column 20, Lines 8-11 and Figure 14, Element 124 and Figure 15, Element 146] that receives data from the inputs [Figure 15, Element 33 and Figure 14, Element 108], stores it and sends it to the respective outputs [Figure 14, Element 32 and Figure 15, Element 144]. The links to the core module/optical core comprise dense wavelength division multiplexed connections, and therefore comprise multiple output/input elements within a single fiber [Figure 14, Elements 128 and 32 and Figure 15, Elements 33 and 16].)

b. Wherein each output device has a plurality of input elements (Figure 4, Element 33, "DWDM Super Packet Link") and a plurality of router output nodes (Figure 4, Element 128) and a respective memory providing said storage for queues of packet data received from the coupling stage and arranged to receive data from all of the said plurality of input elements and arranged to output data to all of said plurality of output nodes (Figure 12b, Super Packet Factory, Element 140 and Fig 15, Element 146). (Both the input device/ingress edge unit and the output device/egress edge unit have a memory forming a queue [Column 20, Lines 8-11 and Figure 14, Element 124 and Figure 15, Element 146] that receives data from the inputs [Figure 15, Element 33 and Figure 14, Element 108] and sends it to the respective outputs [Figure 14, Element 32 and Figure 15, Element 144]. The links to the core module/optical core comprise dense wavelength division multiplexed connections, and therefore comprise multiple output/input elements within a single fiber [Figure 14, Elements 128 and 32 and Figure 15, Elements 33 and 16].)

For Claim 14, *Miles, et al.* as modified by *Leonski*, et al. discloses a network wherein each packet router has a respective control device connected to its input stage and to its coupling stage for outputting packets to said coupling stage in dependence on routing information carried by packets. . (The packet classification module classifies a packet and assigns information indicative of a router output node to the packet and forewords the packet to the appropriate ingress super packet factory queue based on the assigned output port [Column 27, Lines 38-47 and Column 28, Lines 4-10 and 19-27] from which the packet is aggregated into a super packet and sent by the control device at the appropriate time [Column 21, Line 64 through Column 22, Line 6]. The control device/Super Packet Transmit Controller is connected to the input stage via the super packet ingress aggregator and the partial super packet ingress aggregator [See Figure 14]. The Control Device/Super Packet Transmit Controller is also connected to the core controller/coupling stage [Column 21, Lines 32-35].)

For Claim 17, *Miles, et al.* as modified by *Leonski*, et al. discloses discarding packets in said *input* stages if queues therein overflow (Column 33, Lines 62-67).

Miles, et al. as modified by *Leonski*, et al. does not disclose discarding packets in said output stages if queues therein overflow (Column 33, Lines 62-67). However, in light of the disclosure of ingress packet dropping by *Miles, et al.* as modified by *Leonski*, et al. it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention that if their was an overflow in the output stage buffer, the excess packets could be discarded. Output overflow discarding can be modified/implemented into the system of *Miles, et al.* as modified by *Leonski*, et al. by discarding received packets over the output stage queue size. The motive to implement Output overflow discarding in the system of *Miles, et al.* as modified by *Leonski*, et al. is to allow room for new packets when an overload occurs.

For Claim 18, *Miles, et al.* as modified by *Leonski*, et al. discloses the coupling stage of at least the first packet router is arranged to optically couple the input stage of the first packet router to the output stage of the first router. (Figure 4, Elements 30, 23, 33, 60, 70 and 160) Column 11, Line 1-36).

For Claim 19, *Miles, et al.* as modified by *Leonski*, et al. discloses said coupling stage is arranged to provide free-space connections. (Figure 4, Elements 30, 23, 33, 60, 70 and 160) Column 11, Line 1-36).

9. **Claims 15-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over unpatentable Miles, et al. (US Patent No. 6,665,495 B1) and *Leonski*, et al. (US Patent No. 6,990,063) as applied to claim 12 above, and further in view of *Dell*, et al. (US Pre Grant Publication No. 2002/0075883).

For Claim 15, *Miles, et al.* as modified by *Leonski*, et al. discloses a management device connected to receive information on the size of queues in each said *input* device. (Column 22, Lines 60-67).

Miles, et al. as modified by *Leonski*, et al. does not disclose, but *Dell*, et al. discloses that a management device is connected to receive information on the size of queues in each said output device (Figure 1, Output Processors 1-64, Arbitration Logic 820 and Paragraph 0086). (The individual output processors transmit the status of their output processors to the arbitration logic, which controls the flow of packets through the crossbar by issuing grants. [Paragraph 0086].) Thus it would have been obvious to a person of ordinary skill in the pertinent art that the queue status reporting of *Dell*, et al. could be included in the router of *Miles, et al.* as modified by *Leonski*, et al. The queue status reporting of *Dell*, et al. can be modified/implemented into the

router of *Miles, et al.* as modified by *Leonski*, et al. by having the egress super packet factory report buffer status to the optical core controller in the same way as the ingress super packet factory of *Miles, et al.* as modified by *Leonski*, et al. The motive to combine the queue status reporting of *Dell*, et al. with the router of *Miles, et al.* is provided by *Dell*, et al. and is to prevent the transmission of data to output devices that are congested [Paragraph 0131].

For Claim 16, *Miles, et al.* as modified by *Leonski*, et al. and *Dell*, et al. discloses the management device is connected to each control device for modifying routing tables in accordance with queue size information. (Figure 5, Elements 44-46 and Element 38 and Column 22, Lines 60-67). (The control packet processor/congestion management routines take into account the congestion/input buffer status of the ingress edge unit and modifies the switching/routing pattern to increase the bandwidth allocated to high traffic nodes [Column 22, Lines 60-67 and Column 33, Lines 60-64].)

Miles, et al. as modified by *Leonski*, et al. do not disclose that the management device is connected to each control device for modifying routing tables in accordance with *output device* queue size information. *Dell*, et al. discloses altering switching/routing patterns in accordance with queue size information. (Figure 1, Output Processors 1-64, Arbitration Logic 820 and Paragraph 0086). (The individual output processors transmit the status of their output processors to the arbitration logic, which controls the flow of packets through the crossbar by issuing grants, and restricts or halts the flow of packets to output devices with full buffers. [Paragraph 0086]). Thus, it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to combine the output port based routing of *Dell*, et al. with the system of *Miles, et al.* as modified by *Leonski*, et al. and *Dell*, et al. The output port based routing of *Dell*, et al. can be modified/implemented into the system of *Miles, et al.* as modified by *Leonski*, et al. and *Dell*, et al. by adjusting the slot routing table of *Miles, et al.* as

modified by *Leonski*, et al. and *Dell*, et al. to decrease the traffic flow to output devices that have full buffers. The motive to combine the output port based routing of *Dell*, et al. with the system of *Miles, et al.* as modified by *Leonski*, et al. and *Dell*, et al. is provided by *Dell*, et al. and is to prevent the transmission of data to output devices that are congested [Paragraph 0131].

10. **Claim 31** is rejected under 35 U.S.C. 103(a) as being unpatentable over Miles, et al. (US Patent No. 6,665,495 B1) and Li, et al. (US Pre Grant Publication No. 2004/0066799 A1) as applied to claim 21 above, and further in view of *Moriwaki*, et al. (US Patent No. 6,999,413).

For Claim 31, *Miles, et al.* as modified by *Li*, et al. does not disclose but *Moriwaki*, et al. from the same or similar field of endeavor, discloses a packet router wherein the number of spatially separate paths provided by said coupling stage is greater than the number of inputs to said input stage (Figure 1, Line I/F #1 has multiple spatially separate crossbar connections [10-1 to 10-n] to its single input). Thus, it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to include the multiple parallel crossbars of *Moriwaki*, et al. in the system of *Miles, et al.* as modified by *Li*, et al. and *Battle,* et al. The multiple parallel crossbars of *Moriwaki*, et al. can be modified/implemented into the system of *Miles, et al.* as modified by *Li*, et al. and *Battle,* et al. by installing and connecting to each ingress and egress module multiple parallel cross bar matrixes such that the number of crossbar matrixes exceeds the number of inputs to each ingress module. The motive to combine the multiple parallel crossbars of *Moriwaki*, et al. with the system of *Miles, et al.* as modified by *Li*, et al. and *Battle,* et al. is provided by *Moriwaki*, et al. and is to allow for high capacity, expandability and fault tolerance (*Moriwaki*, Column 3 Lines 45-67).

Miles, et al. as modified by *Li*, et al., *Battle,* et al. and *Moriwaki*, et al. does not disclose that multiple parallel crossbars can be used in a multi stage switch where the number of inputs to an ingress edge module/Line I/F exceed one. However, it is officially noted that the use of multi stage switches was well known in the pertinent art at the time of the invention. Thus, it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention that multiple parallel crossbars exceeding the number of inputs could also be used in a multi stage switch where the ingress edge module/Line I/F has multiple inputs. Therefore, claim 10 would have been obvious because the technique for improving switches by installing multiple parallel crossbars exceeding the inputs to the ingress edge unit was part of the ordinary capabilities of a person of ordinary skill in the art, in view of the teaching of the technique for improvement in other situations.

Miles, et al. as modified by *Li*, et al., *Battle,* et al. and *Moriwaki*, et al. does not disclose that the ingress edge unit and core switch of *Moriwaki*, et al. could be optic. However, it is officially noted that the use of fiber optic cross ingress edge units and optical core switches was well known in the pertinent art at the time of the invention. Thus, it would have been obvious to a person of ordinary skill in the pertinent art to combine fiber optic cross ingress edge units and optical core switches with the system of *Miles, et al.* as modified by *Li*, et al. and *Moriwaki*, et al. Fiber optic cross ingress edge units and optical core switches can be modified/implemented into the system of *Miles, et al.* as modified by *Li*, et al. and *Moriwaki*, et al. by converting the cross point matrix to an optical cross point matrix. Thus, implementing a optic cross point matrix in the cross point matrix of into the system of *Miles, et al.* as modified by *Li*, et al. and *Moriwaki*, et al. would have been obvious because the known technique of implementing a fiber optic switching matrix in place of a switching matrix was recognized as part of the ordinary capabilities of one skilled in the art.

11. **Claim 32** is rejected under 35 U.S.C. 103(a) as being unpatentable over Miles, et al. (US Patent No. 6,665,495 B1) and Li, et al. (US Pre Grant Publication No. 2004/0066799 A1) as applied to claim 21 above, and further in view of *Leonski*, et al. (US Patent No. 6,990,063).

For Claim 32, *Miles, et al.* discloses a method comprising:

a. A router holding queues of enhanced packet data (Figure 14, Element 124) prior to issue to said coupling stage (Figure 14, Elements 126, 128 and 32).

b. A router holding queues of packet data received from the coupling stage (Figure 15, Element 146 and Elements 33, 136 and 138).

c. A router locating an egress edge unit and the corresponding enhanced packet data queue separate from the router (Column 25, Lines 50-61).

Miles, et al. and *Li*, et al., do not disclose the existence of a second router. However, the cascading of multiple routers was well known in the pertinent art at the time of the invention. Thus it would have been obvious that the remote output of a first router as described by *Miles,* et al. as modified by *Li*, et al. as presented in claim 22 above could be connected to the remote input of a second router as described by *Miles,* et al. as modified by *Li*, et al. as presented in claim 22 above, thus giving the structure described by claim 32, with the exception of the existence of an output queue of packet data in the output device of the first router that is connected to the input device of the second router. A second router as described by *Miles,* et al. can be connected to a first router as described by *Miles,* et al. by connecting the remote output of the first router *Miles,* et al. to the input of a second router as of *Miles*, et al. The motive to combine a second router as described by *Miles,* et al. with a first router as described by *Miles,* et al. is to allow the use of multiple packet switches, therefore increasing bandwidth and the number of reachable destinations.

Miles, et al. and *Li*, et al., do not disclose, but *Leonski*, et al., from the same or similar field of endeavor discloses that the *input* device of the second router (Figure 1a, Element 115) does not have a holding queue (Figure 3B, Showing no input queue in SE-2) but the output device of the first router (Figure 1A, Element 110) does posses a holding queue (Figure 3A, Element 320). (The first packet router/SE-1 takes input packets and distributes packets destined for the appropriate SE-2 stage/second router to an output queue [Figure 3A, Element 320] for that stage. The output of that output stage queue is then sent to the distribution stage of the SE-2/second router [Figure 3A, Elements 320, 325 and 328].) Thus it would have been obvious to a person of ordinary skill in the pertinent art that the single buffered router connection of *Leonski*, et al. could be combined with the system of *Miles, et al.* The single buffered router connection of *Leonski*, et al. can be modified/implemented into the system of *Miles, et al.* by removing the input buffer from the second router input stage that is connected to the remote first router output stage. The claim would have been obvious because the substitution of the known element of a buffered router input stage for the element of an un-buffered router input stage would have been recognized by one of ordinary skill in the pertinent art at the time of the invention to yield the predictable result of cascaded routers connected by an un-buffered input.

Miles, et al. and *Li*, et al., and *Leonski*, et al. do not disclose that the *output* device of the first router (Figure 1a, Element 115) does not have a holding queue (Figure 3B, Showing no input queue in SE-2) but the *input* device of the second router (Figure 1A, Element 110) does posses a holding queue (Figure 3A, Element 320). However, a person of ordinary skill in the pertinent art at the time of the invention would have recognized that the output queue in the output device of the first router could be moved to the input queue of the input device of the second router to achieve the same buffering effect. Queue relocation can be modified/implemented into the system of *Miles, et al.* as modified *Li*, et al., and *Leonski*, et al. by

moving the super packet factory and super packet processors [Figure 12b, Elements 140 and 150] the from the egress edge unit/output device of the first router of *Miles, et al.* as modified *Li*, et al., and *Leonski*, et al. to the input device of the second processor. The motive to combine queue relocation with the system of *Miles, et al.* as modified *Li*, et al., and *Leonski*, et al. is to allow the simplification of the components of the egress edge unit/output device.

12. **Claim 33** is rejected under 35 U.S.C. 103(a) as being unpatentable over Miles, et al. (US Patent No. 6,665,495 B1) and Li, et al. (US Pre Grant Publication No. 2004/0066799 A1) as applied to claim 21 above, and further in view of *Dell*, et al. (US Pre Grant Publication No. 2002/0075883).

For claim 33, *Miles,* et al. as modified by Li, et al. discloses providing information on the size of queues of data *sent to* said coupling stage, and using said information to effect changes on routing information (Column 22, Lines 60-67 and Figure 5, Elements 44-46 and Element 38 and Column 22, Lines 60-67). (The control packet processor/congestion management routines take into account the congestion/input buffer status of the ingress edge unit and modifies the switching/routing pattern to increase the bandwidth allocated to high traffic nodes [Column 22, Lines 60-67 and Column 33, Lines 60-64].)

Miles, et al. as modified by Li, et al. does not disclose but *Dell*, et al., from the same or similar field of endeavor discloses providing information on the size of queues of data *sent to* said coupling stage, and using said information to effect changes on routing information (Figure 1, Output Processors 1-64, Arbitration Logic 820 and Paragraph 0086). (The individual output processors transmit the status of their output buffers to the arbitration logic, which controls the flow of packets through the crossbar by issuing grants, and restricts or halts the flow of packets

to output devices with full buffers. [Paragraph 0086]). Thus, it would have been obvious to a person of ordinary skill in the pertinent art at the time of the invention to combine the output port based routing of *Dell*, et al. with the system of *Miles, et al.* as modified by *Leonski*, et al. and *Dell*, et al. The output port based routing of *Dell*, et al. can be modified/implemented into the system of *Miles, et al.* as modified by *Leonski*, et al. by having the control packet processor/congestion management device of *Miles,* et al. (Figure 5, Elements 44 and 46) adjust the slot routing table of *Miles, et al.* as modified by *Leonski*, et al. and *Dell*, et al. to decrease the traffic flow to output devices that have full buffers based on buffer fill information received from the egress edge modules. The motive to combine the output port based routing of *Dell*, et al. with the system of *Miles, et al.* as modified by *Leonski*, et al. and *Dell*, et al. is provided by *Dell*, et al. and is to prevent the transmission of data to output devices that are congested [Paragraph 0131].

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher M. Crutchfield whose telephone number is (571) 270-3989. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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